Claims

[c1] What is claimed is:

A method of reducing electrical noise coupling to a noise-sensitive chip input signal, comprising the steps of:

providing input circuitry including a noise isolated transformer;

converting a noise-sensitive chip input signal to an intermediate signal using said transformer;

converting said intermediate signal to a converted signal having a voltage level compatible with that of a predetermined logic level using auxiliary noise-isolated support circuitry; and

using said converted signal as input to intended on-chip destination circuitry.

[c2] 2.A method according to claim 1, wherein said steps of converting a noise-sensitive chip input signal is performed using a monolithic integrated transformer.

[c3] 3.A method according to claim 1, wherein said step of converting the transformed signal is performed using a biased receiver transistor network having a PFET current mirror coupled with a NFET current mirror.

[c4] 4.A method according to claim 1, wherein said input signal in said step of converting a noise-sensitive chip input signal originates in a first voltage domain and said intermediate signal in said multiplying step is output to a second voltage domain, said second voltage domain being noncontiguous with said first voltage domain.

[c5] 5.A method according to claim 1, wherein said input signal in said step of converting a noise-sensitive chip input signal originates at an off-chip signal source and is output to an on-chip signal sink included in on-chip analog circuitry.

[c6] 6.A method according to claim 5, wherein said off-chip signal source is a reference clock.

[c7] 7.A method according to claim 1, wherein said converted signal in said multiplying step is input to a PLL.

[c8] 8.An integrated circuit designed to reduce on-chip noise coupling, the integrated circuit comprising:
a circuit transformer capable of converting a noise sensitive input signal to an output signal having a voltage compatible with a predetermined sink voltage logic level; and
a biased receiver transistor networkhaving a PFET current mirror coupled with a NFET current mirror, said biased

receiver transistor network designed to multiply said transformer output signal to offset a mutual coupling loss of said transformer.

[c9] 9.An integrated circuit according to claim 8, wherein said input signal originates in a first voltage domain and said output signal from said biased receiver transistor network is output to a second voltage domain, said second voltage domain being noncontiguous with said first voltage domain

[c10] 10.An integrated circuit according to claim 8, wherein said input signal originates at an off-chip signal source and is output to an on-chip signal sink included in on-chip analog circuitry.

[c11] 11.An integrated circuit according to claim 10, wherein said off-chip signal source is a reference clock.

[c12] 12.An integrated circuit according to claim 8, wherein said output signal from said biased receiver transistor network is input to a PLL

[c13] 13.An integrated circuit according to claim 8, wherein said transformer is a monolithic integrated transformer.

[c14] 14.An integrated circuit designed to reduce on-chip noise coupling, the integrated circuit comprising:

means for converting a noise sensitive input signal to an output signal having a voltage compatible with a predetermined sink voltage logic level; and
means for multiplying said transformer output signal to offset a mutual coupling loss of said transformer.

[c15] 15.An integrated circuit according to claim 14, wherein said means for converting is a circuit transformer.

[c16] 16.An integrated circuit according to claim 15, wherein said circuit transformer is a monolithic integrated transformer.

[c17] 17.An integrated circuit according to claim 14, wherein said means for multiplying is a biased receiver transistor network having a PFET current mirror coupled with a NFET current mirror.

[c18] 18.An integrated circuit according to claim 17, wherein said input signal originates in a first voltage domain and said output signal from said biased receiver transistor network is output to a second voltage domain, said second voltage domain being noncontiguous with said first voltage domain.

[c19] 19.An integrated circuit according to claim 14, wherein said input signal originates at an off-chip signal source

and is output to an on-chip signal sink included in on-chip analog circuitry.

[c20] 20.An integrated circuit according to claim 19, wherein said off-chip signal source is a reference clock.

[c21] 21.An integrated circuit according to claim 14, wherein said output signal from said biased receiver transistor network is input to a PLL.